Low-Frequency Noise in Bilayer MoS_2 Transistor

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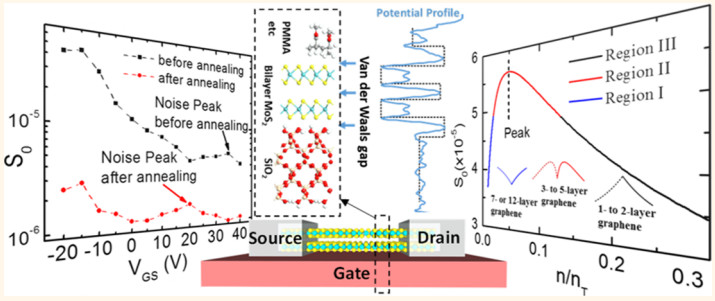
ABSTRACT Low-frequency noise is a significant limitation on the performance of nanoscale electronic devices. This limitation is especially important for devices based on two-dimensional (2D) materials such as graphene and transition metal dichalcogenides (TMDs), which have atomically thin bodies and, hence, are severely affected by surface contaminants. Here, we investigate the low-frequency noise of transistors based on molybdenum disulfide (MoS_2), which is a typical example of TMD. The noise measurements performed on bilayer MoS_2 channel transistors show a *noise peak* in the gate-voltage dependence data, which has also been reported for graphene. To understand the peak, a trap decay-time based model is developed by revisiting the carrier number fluctuation model. Our analysis reveals that the peak originates from the fact that the decay time of the traps for a 2D device channel is governed by the van der Waals bonds between the 2D material and the surroundings. Our model is generic to all 2D materials and can be applied to explain the V, M and Λ shaped dependence of noise on the gate voltage in graphene transistors, as well as the noise shape dependency on the number of atomic layers of other 2D materials. Since the van der Waals bonding between the surface traps and 2D materials is weak, in accordance with the developed physical model, an annealing process is shown to significantly reduce the trap density, thereby reducing the low-frequency noise.



KEYWORDS: 2D material · graphene · low-frequency noise · MoS_2 · van der Waals bond · trap decay time

Recently, atomically layered 2D materials such as graphene,[1,2] MoS_2,[3,4] and WSe_2[5,6] have attracted much attention in the electronics and optoelectronics communities due to their ultrathin (<1 nm) nature and pristine surfaces (free of dangling bonds) that allow excellent electrostatic control for device applications. These 2D materials, in monolayer to few layer, can be mechanically exfoliated from their layered bulk forms[1−6] for prototyping purposes, or synthesized *via* chemical vapor deposition for large-scale manufacturing in the near future.[7−10] Such atomically thin body can also be attractive for highly sensitive sensors[11−13] and ultrascaled high speed electronic devices.[14] However, the low-frequency noise can be a limiting factor in those applications. Low-frequency noise in electronic devices was first discovered in vacuum tubes[15] with the spectral density (S) proportional to $1/f^{\alpha}$, where f is the frequency and α is an empirical coefficient. This type of noise is usually referred to as $1/f$ noise or flicker noise, and the frequency range is usually smaller than few kilohertz (kHz). For sensor applications, the low-frequency noise determines a basic limitation on sensitivity.[16] This is because high-frequency noise (shot noise or thermal noise) can be reduced by averaging when the measurement time is increased. However, it is difficult to improve the accuracy of a system limited by low-frequency noise by increasing the measurement time, since $S \propto 1/f^{\alpha}$ and $t \propto 1/f$.[17,18] For digital electronic device applications, smaller electronic devices usually suffer from larger noise-to-signal ratio;[19,20] hence, low-frequency noise sets the lower limit on the level of signal that can be processed by electronic devices and circuits,[21] thus limiting the further scaling down and minimization of power consumption.[22] For analog electronic device applications, low-frequency noise in the oscillators[23] produces phase noise that limits the wireless channel density[24] and hence reduces the wireless communication quality.[25]

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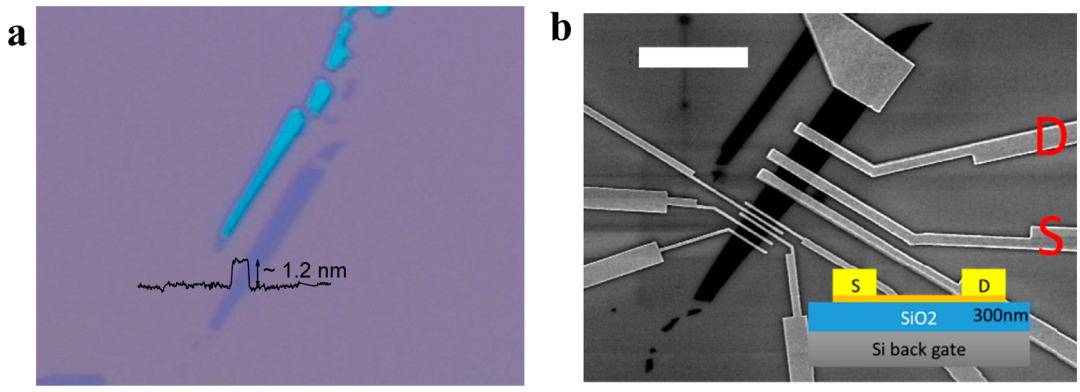

Figure 1. (a) Optical image of exfoliated bilayer MoS_2 on 300 nm SiO_2/Si substrate. The superimposed atomic force microscope (AFM) height profile measurement shows a thickness of 1.2 nm, which coincides with the thickness of bilayer MoS_2.[9](b) Scanning electron microscope (SEM) image showing the top-view of the fabricated devices with electrodes contacting the bilayer MoS_2. The terminals of the device measured in this work are denoted with "S" for source and "D" for drain. Measurements on the other devices are included in the Supporting Information S1. The "white" scale bar denotes 5 μm. The inset shows the schematic cross-sectional view of the fabricated device.

Therefore, detailed investigation of low-frequency noise in 2D materials is necessary for their analog and digital circuit applications. On the other hand, 2D materials do not have surface dangling bonds, so the surface contaminations and the substrate are attached to them *via* van der Waals bonds. The van der Waals bonds have large variation in length/strength and depend on the specific elements, atomic groups, and many other factors.[26,27] Therefore, it is difficult to study all the van der Waals bonds using theoretical calculations. Low frequency noise measurement is essentially the Fourier transform of the time domain telegraph noise measurement, so it can capture the statistics of the charge decay time, which relates to the van der Waals bonds. Hence, low frequency noise could also be a useful tool to study the surface/interface physics of 2D materials. While there has been several reports on the low-frequency noise phenomenon in graphene devices,[28−33] there is only limited work in the case of TMDs,[34−37] which are promising candidates for future nanoelectronic applications. One of the recent works on noise measurement of monolayer MoS_2 transistor states that the noise shows monotonously decreasing trend with increasing gate voltage and can be explained by Hooge's empirical model.[34] Another noise measurement of trilayer MoS_2 transistor[37] indicates that the noise increases as the carrier density increases when the gate voltage is larger than the threshold voltage. However, none of the above works offer a physical model to provide insights into the experimental trends.

In this work, we investigated the low-frequency noise of back-gated bilayer MoS_2 field-effect-transistors (FET) and studied their noise performance as a function of gate voltage as well as temperature. The presence of a *noise peak* in the linear region (*i.e.*, gate voltage is larger than threshold voltage and drain-to-source voltage is smaller than effective gate voltage) is reported for the first time in the case of MoS_2 FETs. To provide physical insights into this phenomenon, we examine the noise models and show that the decay-time distribution of the traps in the McWhorter's model (carrier number fluctuation model)[38] can be used to explain the peak. We demonstrate that this model can also be used to explain the "V" shaped, "M" shaped, or "Λ" shaped gate-voltage dependence of noise reported previously[28−33,39−41] in case of graphene. Moreover, we analyze the effect of annealing on the noise performance of bilayer MoS_2 FETs and show that noise can be significantly reduced through annealing in such atomically thin channel materials.

RESULTS

In our study, we chose the bilayer MoS_2 as the platform to study the noise performance of 2D materials, since the bilayer MoS_2 FET offers significantly smaller metal contact resistance compared with monolayer MoS_2 FET with Ti contact (740 k$\Omega\cdot\mu$m for monolayer, 15.6 k$\Omega\cdot\mu$m for bilayer MoS_2)[6] while retaining most of the benefits and characteristics of 2D materials. As indicated in Figure 1, the MoS_2 flake is mechanically exfoliated from bulk crystal onto 300 nm silicon dioxide grown on silicon, which provides good optical contrast.[42] The thickness of the flake is further confirmed using AFM measurement to be approximately 1.2 nm, which is the reported thickness of bilayer MoS_2.[9] Subsequently, 30 nm titanium followed by 100 nm gold are patterned on top of the sample to form the source and drain electrodes, and the highly n-doped silicon substrate is used as the back gate. (The details about device fabrication are included in the Methods section).

The output ($I_{DS} - V_{DS}$) and input ($I_{DS} - V_{GS}$) characteristics of the fabricated FET are shown in Figure 2, a and b, respectively. Due to the large bandgap (1.8 eV for monolayer and 1.6 eV for bilayer)[43] of MoS_2, most metals form Schottky contacts[44] with it, which is also

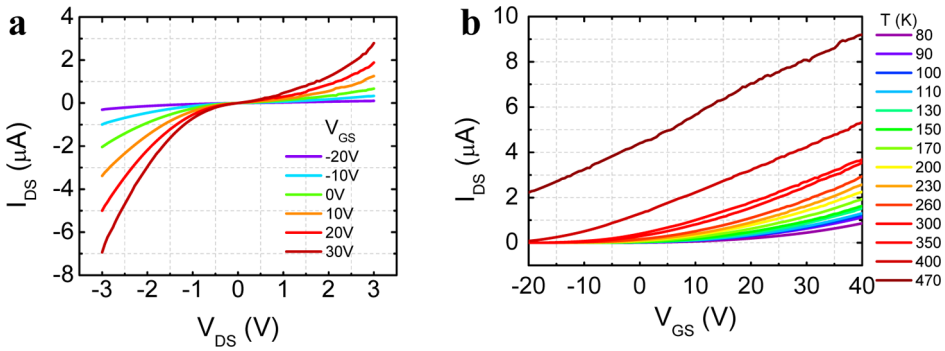

Figure 2. (a) Drain current (I_{DS}) as a function of drain voltage (V_{DS}) at room temperature for different gate voltages (V_{GS}), showing the nonlinear Schottky contact between MoS_2 and metal. (b) Drain current (I_{DS}) as a function of gate voltage (V_{GS}) at different temperatures for V_{DS} = 3 V.

reflected in Figure 2a by the nonlinear behavior of $I_{DS}-V_{DS}$ plot. A general model, which takes into account the noise distribution contributed by the contact as well as by the channel can be expressed as[45]

$$\frac{S_I}{I^2} = \eta^2 \frac{S_{RSB}}{R_{SB}^2} + (1-\eta)^2 \frac{S_{RC}}{R_C^2} \quad (1)$$

where S_I is the current noise power spectral density, I is the corresponding DC current, S_I/I^2 denotes the noise-to-signal ratio, $\eta = R_{SB}/(R_C + R_{SB})$, R_{SB} is the Schottky junction's resistance, R_C is the channel's resistance, S_{RSB} is the noise power density ("noise" for short) contributed by the Schottky junction, and S_{RC} is the noise contributed by the channel. When the gate voltage is larger than the threshold (V_T) and $V_{DS} < V_{GS} - V_T$ (linear region), $R_C \gg R_{SB}$[4] (the contact resistance and channel resistance calculations are included in the Supporting Information S2), hence, $\eta \to 0$, and eq 1 reduces to S_{RC}/R_C^2, indicating that the channel noise dominates. Therefore, the noise performance in the linear region reflects the MoS_2 channel's noise behavior.

The measured noise data is shown in Figure 3 (the noise measurement setup is described in the Supporting Information S3). As shown in Figure 3a, the current noise power spectral density $S_I(f)$ follows $1/f$ trend. The actual frequency index α is extracted by fitting the $S_I(f)$ to $1/f^{\alpha}$. As shown in Figure 3b, the α is around 1 and the S_I is proportional to I_{DS}^2. So S_I can be expressed as $S_0 I_{DS}^2/f$, where S_0 is a dimensionless parameter that characterizes the magnitude of the noise. To compare the noise in different measurements and reduce the measurement error at specific frequencies, S_0 is evaluated by[40,46]

$$\overline{S_0} = (1/N) \sum_{m=1}^{N} f_m S_{Im}/I_m^2 \quad (2)$$

where N is the number of the frequency points at which noise is measured, f_m, S_{Im}, and I_m are the frequency value, current noise spectral density, and DC current, respectively. Figure 3c summarizes the values of S_0 at different gate voltages and temperatures, where the white dots denote the threshold voltages for a given temperature. The threshold voltage values are extracted from the $I_{DS}-V_{GS}$ curves in Figure 2b by linear extension of the data in the range of 30 V < V_{GS} < 40 V, where all the data are in the linear region, and by taking the intercept with the x-axis as the threshold voltage.[47] In other words, the noise data above the white dots (in Figure 3c) are in the linear region, and mainly contributed by the MoS_2 channel, as the contact resistance is low in this region.

It is interesting to note that the noise peaks can be observed at certain gate voltages in the linear region, as shown in Figure 4, and these peaks are repeatable in other bilayer MoS_2 devices as shown in the Supporting Information S1. The noise peak in the linear region is unexpected compared to a previous report on monolayer MoS_2 transistor,[34] but it is similar to the "M"-shaped gate voltage dependence of noise observed in graphene transistors.[28−33]

DISCUSSION

To explain the noise dependence on the gate voltage in our measurements, we revisited the carrier number fluctuation model and developed a trap-decay-time based model to qualitatively explain the measurement results and provide physical insight into the noise source in 2D materials based electronic devices. Another well-known low frequency model is the mobility fluctuation model[38] or Hooge's model. However, it is not suited to this case (*i.e.*, monolayer or few layer 2D materials with large surface-to-volume ratio and large number of interface traps) and further discussion is provided in the Supporting Information S5. In the carrier number fluctuation model, $1/f$ noise is the collection of generation and recombination noise, which is known to have a noise power spectral density of[48]

$$S_I(\omega) = 4\overline{\delta I^2} \int_{\tau_1}^{\tau_2} g(\tau) \frac{\tau}{1+(\omega\tau)^2} d\tau \quad (3)$$

where δI is the change in current induced by the capture or emission of a carrier by a trap, τ is the decay time of traps, τ_1 and τ_2 represent the low and high boundary of trap's decay time, $\omega = 2\pi f$, $g(\tau) = 1/\ln(\tau_2/\tau_1)(1/\tau)$ is the trap density assuming the traps are uniformly distributed in space and energy.

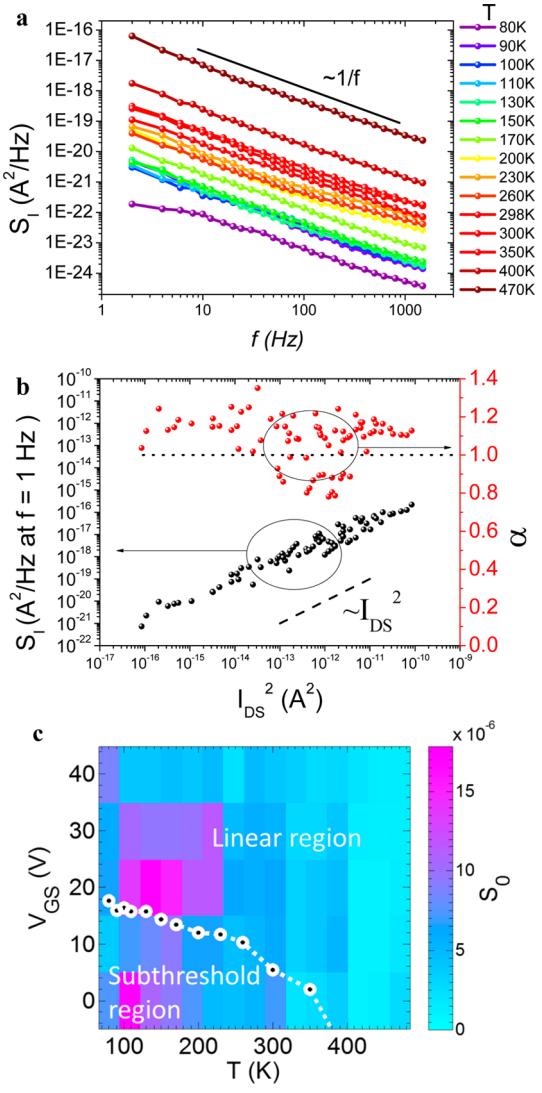

Figure 3. (a) The current noise power spectral density data measured at different temperatures with $V_{GS} = 0$ and $V_{DS} = 3$ V. The dashed line shows the slope of the 1/*f* noise, which indicates that all the data follow 1/*f* trend. The current noise power spectral density data for other values of V_{GS} are included in the Supporting Information S4. (b) Current noise power spectral density S_I and α index extracted from the noise power spectral density data for all values of V_{GS} and temperature. The data corresponding to the left axis is the current noise power spectral density S_I at $f = 1$ Hz, where the dashed line shows the I_{DS}^2 line, which indicates that the noise power is proportional to I_{DS}^2. The data corresponding to the right axis is the α index, which is extracted by fitting the data to $1/f^{\alpha}$, where the dotted line shows $\alpha = 1$. (c) S_0 (calculated using eq 2) at different gate voltages and temperatures for $V_{DS} = 3$ V. The white dots and dashed curve denote the threshold voltages, and the region below the white dots represents the subthreshold region, while the region above the white dots represents the linear region.

The normalized noise power spectral density $S(\omega)$ can be estimated by[48]

$$S(\omega) = \frac{S_I(\omega)}{I^2} = \frac{4\delta I^2}{I^2} \frac{\tan^{-1}(\omega\tau_2) - \tan^{-1}(\omega\tau_1)}{\omega \ln(\tau_2/\tau_1)} \quad (4)$$

where the first term, $\delta I^2/I^2$, is a dimensionless constant. If $\tau_1 \ll 1/\omega \ll \tau_2$, it implies that the trap decay time has wide distribution, and eq 4 becomes proportional to $1/\omega$.

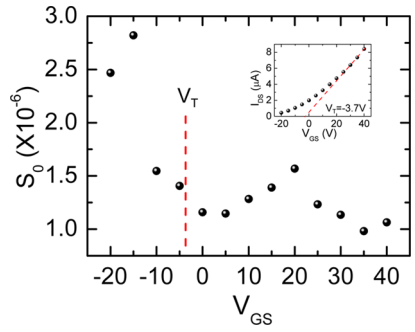

Figure 4. Typical noise dependency on gate voltage measured at room temperature with $V_{DS} = 3$ V (This device is the same device measured in Figure 3 but annealed. The noise peak becomes more distinct after annealing. The effect of annealing is discussed later and shown in Figure 7). The inset shows the threshold voltage (V_T) extraction from the $I_{DS}-V_{GS}$ curve. For gate voltages smaller than the threshold voltage, the Schottky contact dominates the noise. Since the Schottky resistance reduces as the gate voltage increases, the noise reduces with gate voltage. For gate voltages larger than the threshold voltage, the channel noise dominates. The noise shows a *peak* at certain gate voltage, which is similar to graphene's "M" shaped noise data reported in several works.[28−33]

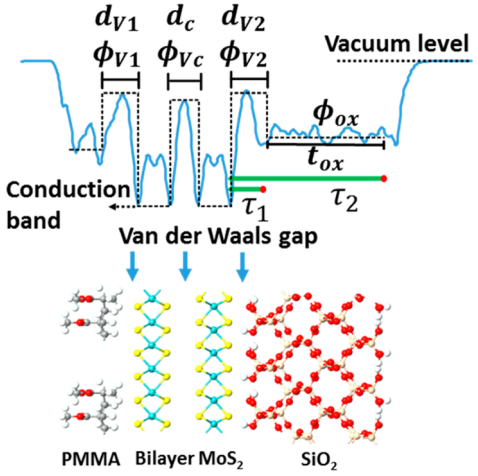

Figure 5. The energy diagram and the corresponding spatial schematic illustrating the cross section of the device channel made from bilayer MoS_2. The underlying blue curve is the effective potential calculated by density functional theory (DFT) assuming the PMMA as surface contaminants (surface traps). MoS_2 forms van der Waals bond with the top surface traps and the substrate, so that the trap decay time for the traps in the PMMA or SiO_2 is enlarged by the van der Waals barriers. The black dashed line is the simplified potential barrier, and the potential heights are with respect to the conduction band of MoS_2. d_{v1} and d_{v2} are the van der Waals bond lengths between channel and the PMMA and the SiO_2 surface, respectively, and ϕ_{V1} and ϕ_{V2} are the corresponding barrier heights. d_c is the van der Waals bond length between adjacent MoS_2 layers, ϕ_{Vc} is the corresponding barrier height. τ_1 and τ_2 represent the lower and upper bounds of the decay time of the traps in substrate.

But for 2D materials, $\tau_1 \ll 1/\omega$ may not be true due to higher τ_1 in these materials as explained below, and hence, the τ_1 and τ_2 need careful interpretation.

The energy diagram and the corresponding spatial schematic showing the surroundings and the 2D

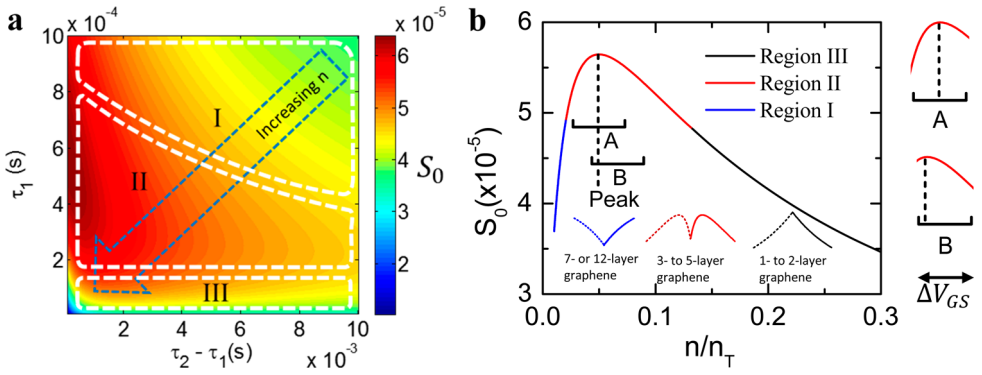

Figure 6. (a) Calculated S_0 contour plot as a function of τ_1 and τ_2. Note that $\tau_2 - \tau_1$, which is the variation range of the charge decay time, is plotted on the *x*-axis, since τ_2 is larger than τ_1. As shown in eq 6, as the carrier density increases, the $\tau_0(n)$ decreases, thus leading to simultaneous decreasing of τ_1 and $\tau_2 - \tau_1$, thereby the noise moves from upper right corner to lower left corner. Although the range of $\tau_2 - \tau_1$ is larger than 0.5 s (as discussed in the Supporting Information S7), for the convenience of labeling, it is limited to 10^{-2} s. (b) S_0 as a function of carrier density corresponding to the cross section along the arrow in (a). The vertical dashed line locates the peak. The brackets "A" and "B" that represent two different devices with different ranges in the variation of n/n_T, correspond to the same variation ranges in V_{GS}. It can be observed that the crossing point of the bracket B with the vertical dashed line (peak value of S_0) is closer to the left-edge of bracket B. Referring to the sketch on the right, if the left-edges of the brackets A and B correspond to the same gate voltage, since the carrier density (n) is proportional to $V_{GS} - V_T$, the gate voltage at the noise peak in device A is larger than that in device B. The insets show the "V", "M", and "Λ" shaped noise data for graphene transistors, corresponding to the three regions as shown in the main plot, where the dashed parts are symmetric to the solid parts with respect to the Dirac points.

semiconductor channel are illustrated in Figure 5. Since the surface of MoS_2 is saturated by sulfur atoms, there are no dangling bonds to form covalent bonds with the surface and substrate traps. Hence, the traps around the channel are separated from the channel by van der Waals gaps, which form potential barriers as illustrated by the effective potential calculated by DFT, where the effective potential of an electron represents its interaction with other electrons and the external electrostatic field (the details about the DFT simulation are described in the Supporting Information S6). According to quantum mechanics, the potential barrier can reduce the electron transfer probability between the traps and MoS_2, which can lead to an increase in trap decay time. The effective potential profiles are simplified to rectangular potential barriers, and the decay time for a carrier to transfer between traps and the channel through a barrier with height ϕ can be expressed by[49,50]

$$\tau(n, d) = \tau_0(n)p(d, \phi) \quad (5)$$

$$\tau_0(n) = \tau_{p0}\left(1 + \frac{n_T}{n}\right) \quad (6)$$

$$p(d, \phi) = e^{2d\sqrt{2m^*\phi}/\hbar} \quad (7)$$

where $\tau_0(n)$ is the decay time when the trap is adjacent to the channel ($d = 0$),[49] which is given by Schottky-Read-Hall statistics.[51] τ_{p0} is a constant, n_T is the trap density, n is the carrier density given by $C_{ox}(V_{GS} - V_T)$ in the linear region, V_T is the threshold voltage. $p(d,\phi)$ is the inverse of the carrier tunneling probability that comes from the Wentzel–Kramers–Brillouin (WKB) theory,[50] which modifies the decay time when the trap is at a distance d apart from the channel, m^* is electron's effective mass, and $\hbar$ is the reduced Planck's constant.

Now, for 3D materials, the traps can form covalent bonds at the channel insulator interface so that the minimum value of d for 3D materials can be 0 and hence, $p(0,\phi) = 1$ and τ_1 is equal to $\tau_0(n)$. But for 2D materials, as illustrated in Figure 5, there is always a van der Waals gap (d_V) between the channel and the interface traps and hence $d \geq d_V$. Using the substrate traps as an example, τ_1 is given by $\tau_0(n)p(d_{V2},\phi_{V2})$ for 2D materials and τ_2 is given by $\tau_0(n)[p(d_{V2},\phi_{V2})p(t_{ox},\phi_{ox})]$, accounting for any traps inside the dielectric substrate (SiO_2).

Various noise phenomena can be explained by this simple model. For this purpose, the $S(\omega)$ is calculated from eq 4 as a function of τ_1 and τ_2 (setting $4\delta I^2/I^2 = 1$) and finally S_0 is calculated from eq 2 using $S(\omega)$ over the frequency range from 1 to 1000 Hz. The effect of τ_1 and τ_2 on S_0 is plotted in Figure 6a. τ_1 and τ_2 are converted to n/n_T by eqs 5–7 assuming $\tau_{p0}p(d_{V2},\phi_{V2})$ and $\tau_{p0}[p(d_{V2},\phi_{V2})p(t_{ox},\phi_{ox})]$ to be 10^{-5} s and 10^{-4} s, respectively, without loss of generality (the numerical values shown here are for convenience of demonstration and discussion, the rigorous numerical values for τ_1 and τ_2 are discussed in the Supporting Information S7). The effect of n on S_0 is plotted in Figure 6b. As the carrier density increases, according to eq 6, the $\tau_0(n)$ decreases, which leads to the simultaneous reduction of τ_1 and $\tau_2 - \tau_1$, so the region of interest in Figure 6a moves from upper-right corner to lower-left corner corresponding to the n/n_T increase from small to large in Figure 6b. For the convenience of discussion, three typical regions are marked on Figure 6. If the variation of τ is in region I, the noise increases as carrier density increases; if it is in region II, the noise experiences a peak as the carrier density increases; if it is in region III, the noise decreases as the carrier density increases. For 3D materials that form covalent bonds with oxide, τ_1 is small due to smaller d as

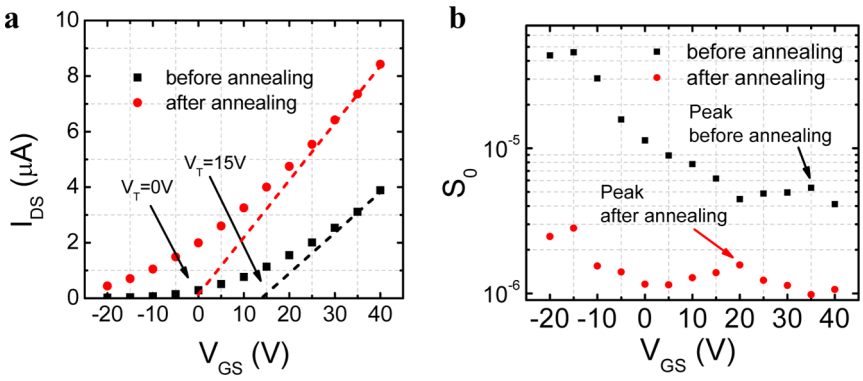

Figure 7. (a) $I_{DS}-V_{GS}$ curve measured for the same device at room temperature with V_{DS} = 3 V before and after annealing. The threshold voltage V_T is around 15 V before annealing, and 0 V after annealing. (b) The noise measured in the same device at room temperature with V_{DS} = 3 V before and after annealing. The noise is 17 times smaller at V_{GS} = −20 V and 3 times smaller at V_{GS} = 40 V after annealing. The noise peak moves to lower gate voltage after annealing.

explained above. Therefore, the noise-τ dependence varies in region III as shown in Figure 6, and hence, the noise decreases as carrier density increases.[52] For 2D materials, d is larger due to the van der Waals bonds; hence, the τ_1 is larger, so it is possible that the noise-τ dependence varies in the upper portion of region III or in either of the other two regions. The interlayer bonding in 2D materials is also van der Waals, so the barrier between atomic planes d_C needs to be taken into account when discussing noise in multilayer 2D materials, and decay time from each atomic plane to the traps needs to be taken into account. Hence, for a 2D channel material with many layers, the noise performance is the superposition of noise from different layers, and the trap decay time is generally larger than that in monolayer channels. Hence, monolayer MoS_2 transistor[34] may work in region III, where the noise in linear region reduces as carrier density increases, while the bilayer MoS_2 transistor in our case may work in region II, where the noise in linear region shows a peak as shown in Figure 4. Similarly, the trilayer MoS_2 transistor[37] may work in region I, where the noise in linear region increases as carrier density increases.

This analysis can also be applied to understand layer number dependence of noise phenomenon in graphene transistors, as illustrated by the inset sketches in Figure 6b. Since graphene's carrier density is proportional to $|V_G - V_{Dirac}|$,[53] the carrier density increases when gate voltage moves away from the Dirac point. In other words the graphene transistor is an ambipolar transistor, and the carrier density is symmetric with respect to the Dirac point. Referring to the Figure 2d of G. Liu's work,[39] the noise in monolayer graphene works in region III, so as $|V_G - V_{Dirac}|$ increases, the carrier density increases, the noise decreases, and the result is symmetric with respect to the Dirac point, so it exhibits a "Λ" shape gate voltage dependence, where the peak point is the Dirac point. On the other hand, due to larger τ_1 and τ_2, 3−5 layer graphene works in region II, so it exhibits an "M" shape gate voltage dependence, where the noise exhibits a peak (suspended monolayer graphene, or supported graphene with dirty substrate can also have larger trap decay time, which may result in "M" shape gate voltage dependence),[29−32] while noise in 7−12 layer graphene due to even larger values of τ_1 and τ_2, works in region I, so it exhibits a "V" shape gate voltage dependence,[39] where the noise increases as the carrier density increases.

To comprehend the effect of temperature on S_0, a comparative measurement is conducted between annealed and unannealed device. As shown in Figure 3c, the noise (S_0) decreases as the temperature increases. Since the traps on the surface are weakly bonded, they can evaporate at high temperatures, under an annealing process conducted as follows. The device is first measured in a vacuum chamber before annealing. Then, the device is heated to 420 K for 20 min and then cooled down in the vacuum chamber to room temperature. Finally, the second measurement is conducted after the annealing process. As shown in Figure 7a, the threshold voltage (V_T) changes from 15 V before annealing to 0 V after annealing, which can be explained by the reduction of trap-induced dipoles in the Schottky junction.[54] In Figure 7b, the noise is 17 times smaller at V_{GS} = −20 V and 3 times smaller at V_{GS} = 40 V; the noise peak moves to a lower gate voltage after annealing. The reduction of noise can arise from the reduction of trap density n_T. The shifting of the noise peak can result from two factors: reduction of V_T as shown in Figure 7a or reduction of n_T. Either phenomenon can make the n/n_T larger in eq 6 for certain V_{GS}. As a consequence, referring to Figure 6b, in region II, after annealing, the device's $S_0 - n/n_T$ relation moves from range A to range B, and therefore, it requires less change in V_{GS} (=Δ V_{GS}, as illustrated by the sketches to the right of the plot in Figure 6b), to reach the peak, so the noise peak for the annealed device occurs at lower V_{GS}. In summary, annealing is an effective way to reduce the surface traps in 2D materials, thereby significantly reducing the noise.

CONCLUSIONS

In conclusion, this paper presented a detailed analysis of low-frequency noise in bilayer MoS_2 transistor.

Noise characteristics as a function of different back gate voltages and temperatures were studied. The analysis suggests that the 2D materials, such as graphene and MoS_2, have longer trap decay times due to the presence of van der Waals bonds compared to 3D materials such as silicon, which can lead to different noise dependencies on carrier density. This work presented a physical model that can explain the observed peaks of low-frequency noise in bilayer MoS_2 transistor as a function of the gate bias voltages. The model can also account for the layer number dependency of the noise behavior. The formulated model is general in its applicability to 2D crystals and can also explain the previously inexplicable V, M and Λ shaped noise peaks in the noise-gate-voltage dependence in graphene devices with different number of layers. Moreover, consistent with the physical interpretation of the model, it is shown that the traps on the surface of 2D materials can be reduced by annealing the device in vacuum, thereby significantly reducing the low-frequency noise.

METHODS

Bilayer MoS_2 flakes were prepared by mechanical exfoliation of bulk MoS_2 (SPI Instrument, Inc.) on 300 nm SiO_2/Si (highly n-doped) substrate. The source and drain regions were defined by electron-beam lithography followed by metallization with PMMA as the photoresist. Subsequently, 100 nm Au film was deposited after a 30 nm Ti film deposition in an electron beam evaporator at 8×10^{-7} mbar. All DC measurements were performed in vacuum (1×10^{-6} mbar) at room temperature after annealing at 420 K for 2 h to remove any absorbed moisture or solvent molecules.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Noise peak data in other devices, details of contact resistance extraction, noise measurement setup, current noise power spectral density for different gate voltages and temperatures, discussion about the mobility fluctuation model, density functional theory (DFT) simulation, and discussion about the numerical values of τ_1 and τ_2. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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